REMARKS

The application has been carefully reviewed in light of the Office Action dated June 7, 2004. Claims 2, 3 and 9 have been amended. Claims 2-4, 8-10, 14 and 17-19 remain pending in this case.

Claims 7 and 9 stand rejected under 35 U.S.C. § 112, for insufficient antecedent basis. Claim 7 has been previously canceled and therefore the rejection is not applicable to claim 7. Claim 9 has been amended and is in full compliance with § 112.

Claims 2, 3, 4, 8-10, 14 and 17-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Wilford et al. (U.S. Patent No. 6,721,233). Applicant respectfully traverses the rejection and requests reconsideration.

Claim 2 recites a method of reading a plurality of N data bits of a data burst comprising "storing said N data bits at respective memory locations . . . such that a preceding data bit of [a] burst is electrically closer to a multiplexer than a next subsequent data bit of said burst." [Emphasis added.]

Wilford fails to teach or suggest this limitation of claim 2 and, what is more, the Office Action fails to even address this language of claim 2. At least for these reasons, claim 2 is allowable over Wilford.

Claim 3 recites a method of storing a plurality of data bits comprising "transferring . . . first and second data bit values to first and second multiplexer locations respectively." [Emphasis added.]

Wilford fails to teach or suggest this limitation of claim 3. While the Office Action purports to address this limitation, it does not point to any portion of Wilford supposedly disclosing the limitation. At best, Wilford discloses that multiplexing circuitry between storage circuitry and buffer circuitry sequentially transfers X sequential data portions between the storage circuitry and the buffer circuitry. Wilford at column 3, lines

18-21. Wilford is silent as to first and second multiplexer locations. At least for these reasons, claim 3 is allowable over Wilford.

Claim 4 recites a method of recovering data comprising outputting a respective plurality of bits from a respective multiplexer input location in a particular time sequence "such that a first bit output is a bit retrieved from one of a plurality of memory locations electrically closest to [a] respective buffer location." [Emphasis added.] Wilford fails to teach or suggest this limitation of claim 4 and, what is more, the Office Action fails to even address this language of claim 4. At least for these reasons, claim 4 is allowable over Wilford.

Claim 8 recites a memory integrated circuit device comprising a plurality of connecting paths each "having a characteristic electrical length." Claim 8 also recites that "the path of said plurality having a shortest electrical length being switchingly connected to [a] first multiplexer input. [Emphasis added.] Wilford fails to teach or suggest this limitation of claim 8 and, what is more, the Office Action fails to even address this language of claim 8. At least for these reasons, claim 8 is allowable over Wilford.

Claim 14 recites a memory integrated circuit device comprising "a plurality of electrical connections . . . operatively connecting a memory bit storage location . . . to a respective demux storage location." Claim 14 also recites that "an electrical connection operatively connected to [a] first output bit [has] a characteristic electrical length no longer than the characteristic electrical length of any other electrical connection of said plurality of electrical connections." [Emphasis added.] Wilford fails to teach or suggest these limitations of claim 14 and, what is more, the Office Action fails to even address this language of claim 14. At least for these reasons, claim 14 is allowable over Wilford.

Claim 17 recites a serial data output signal comprising first and second memory cells "located at respective first and second electrical distances from [a] multiplexer, said first electrical distance being shorter than said second electrical distance." Wilford fails to teach or suggest these limitations of claim 17 and, what is more, the Office Action fails to

even address this language of claim 17. At least for these reasons, claim 17 is allowable over Wilford.

Claim 19, similar to claim 17, recites a computer processing system comprising a multiplexer and "first and second memory cells at respective first and second electrical distances from said multiplexer, said first electrical distance being shorter than said second electrical distance." Claim 19 also recites that the first and second memory cells are adapted to store "first and second data values respectively." Claim 19 further recites that the first signal is output to a central processing unit "before outputting said second signal, thereby adhering to a fixed burst order."

Wilford fails to teach or suggest these limitations of claim 19 and, what is more, the Office Action fails to even address this language of claim 19. At least for these reasons, claim 19 is allowable over Wilford.

Claims 9 and 10 depend from claim 8. Claim 18 depends from claim 17. Claims 9, 10 and 18 are allowable at least for the reasons mentioned above and also because Wilford fails to teach or suggest the respective inventive combinations defined by claims 9, 10 and 18.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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